

## METHOD FOR REDUCING EXTRINSIC BASE-COLLECTOR CAPACITANCE

This application is a Continuation of application Ser. No. 08/479,739 filed Jun. 7, 1995 now abandoned which is a Divisional of application Ser. No. 08/285,601 filed Aug. 3, 1994, now U.S. Pat. No. 5,525,818 which is a Continuation of application Ser. No. 08/112,009 filed Aug. 25, 1993, now abandoned which is a Divisional of application Ser. No. 07/938,190 filed Aug. 31, 1992 now U.S. Pat. No. 5,298,438.

### FIELD OF THE INVENTION

This invention generally relates to reducing extrinsic base-collector capacitance in bipolar transistors.

### BACKGROUND OF THE INVENTION

Without limiting the scope of the invention, its background is described in connection with the manufacturing of bipolar transistors, as an example.

Heretofore, in this field, in bipolar mesa transistors, the base layer extends outside the area of the active device region to enable contacting of the base. This area is called the extrinsic base region, outside the active device region, and it increases the junction capacitance between the base layer and the layer beneath the base (e.g. the collector, in emitter-up devices).

Since junction capacitance limits the high-frequency performance of bipolar transistors, great effort has been spent on reducing the junction capacitance between the base layer and the layer beneath the base. Accordingly, improvements which overcome any or all of the problems are presently desirable.

### SUMMARY OF THE INVENTION

It is herein recognized that a need exists for a method to manufacture a bipolar transistor which reduces the junction capacitance between the base layer and the layer beneath the base. The present invention is directed towards meeting that need.

Generally, and in one form of the invention, during device fabrication, the layer beneath the base is etched laterally; a selective etch is used so that the base layer itself is not significantly affected. The area of the junction between the base and the underlying layer can be significantly reduced.

The selective etching can be accomplished in at least two ways: by including an epitaxial layer in the layer beneath the base which can be selectively removed during fabrication; or by using a doping-selective etch which, for NPN transistors, removes only N-type material but not P-type material (or vice versa for PNP transistors).

Previous partial solutions include minimization of the base contact area and ion bombardment of the extrinsic base region.

Minimization of the base contact area involves a design tradeoff between base resistance (which improves with increasing contact area) and junction capacitance (which degrades with increasing contact area). In contrast, the invention makes the junction capacitance almost independent of base contact area.

Ion bombardment reduces the effective doping density of the layer beneath the base in the extrinsic base region. At best, this approach insures that the layer is depleted of free carriers, so that the dielectric thickness is increased. For

example, in the case of a conventional emitter-up AlGaAs/GaAs heterojunction bipolar transistor, if ion bombardment is used in the extrinsic base region, then the capacitance  $C$  per unit area in this region is determined by the collector thickness  $t$  and the dielectric constant of collector material (e.g. GaAs):

$$C = \epsilon_{GaAs}/t$$

In contrast, if the current solution is applied to the heterojunction bipolar transistor, the capacitance per unit area in the region is no greater than

$$C = \epsilon_{air}/d$$

where  $d$  is the vertical thickness of the undercut layer and  $\epsilon_{air}$  is the dielectric constant of air. Since  $\epsilon_{GaAs}/\epsilon_{air} \approx 13$  (and the entire collector layer may be undercut if desired, so that  $d=t$ ), the capacitance reduction improvement, compared to the ion bombardment approach, is considerably greater.

An additional advantage of the invention is the improvement of the current gain and base resistance compared to the ion bombardment approach. For emitter-up structures, current gains is improved somewhat because the minority carrier lifetime in the extrinsic base is not degraded. Base resistance is improved because the base layer does not undergo ion bombardment. Also, since the junction capacitances are not significantly affected by base contact area, the contact area can be increased to further reduce base resistance.

This invention would be of great use in, although not limited to, microwave amplification or oscillator applications requiring Heterojunction bipolar transistors (HBT) devices to operate above 20 GHz, since conventional HBTs are usually sufficient at lower frequencies.

This is a method of fabricating a heterojunction bipolar transistor on a wafer. This method can comprise: forming a doped subcollector layer on a substrate; forming a doped collector layer on top of the subcollector layer, the collector layer being doped same conductivity type as the subcollector layer; forming a doped base epilayer on top of the collector layer, the base epilayer being doped conductivity type opposite of the collector layer; forming a doped emitter epilayer, the emitter epilayer being doped conductivity type opposite of the base layer to form the bipolar transistor; forming a doped emitter cap layer on top of the emitter epilayer, the emitter cap layer being doped same conductivity as the emitter epilayer; forming an emitter contact on top of the emitter cap layer; etching of the emitter and emitter cap layers to expose the base layer; forming a base contact on top of the base layer; etching of the base and collector layer to expose the subcollector; selective etching a portion of the collector layer to produce an undercut beneath the base layer; and forming a collector contact on top of the subcollector layer.

Preferably, the collector layer is composed of or contains an AlGaAs layer and the subcollector layer is composed of GaAs and the AlGaAs collector layer is selectively etched to produce the undercut region beneath the base layer.

In one embodiment, the base layer, the emitter layer, and the collector layer are composed of silicon. At least the base layer and emitter layers may be epilayers.

### BRIEF DESCRIPTION OF THE DRAWINGS

The drawings are schematic and the vertical has been exaggerated for clarity.